

REMARKS

35 U.S.C. § 101

The examiner rejected claims 1-7 under 35 U.S.C. § 101 as being directed to a method that lacks a tangible result.

Applicant has amended claim 1 to recite "receiving a packet in the packet processor." Accordingly, the rejection should be withdrawn.

Applicant requests that this rejection under 35 U.S.C. 101 be withdrawn. On October 30, 2008, subsequent to the mailing of the present office action, the Federal Circuit issued a decision in *In re Bilski*. In this case, the Federal Circuit adopted a "machine-or-transformation" test for patentability. Under the test, a process will be patentable if: "(1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing." Claim 1 recites a method that is tied to a packet processor, which is a machine or apparatus. As such, the standard applied by the examiner above, is no longer the correct standard for determining patentable subject matter.

Therefore, Applicant requests that the rejection of claims 1-7 under 35 U.S.C. 101 be withdrawn.

The examiner rejected claims 8-14 under 35 U.S.C. § 101 as being directed to an information carrier. Applicant has amended claim 8 to recite "A computer program product, tangibly embodied in a computer-readable storage medium..." Accordingly, the rejection should be withdrawn.

The examiner rejected claims 15-17 under 35 U.S.C. § 101 as being directed to a scheduler that could be interpreted to one of ordinary skill in the art as software, per se. Applicants have amended claim 15 to recite "A hardware scheduler comprises... a processor configured to schedule processing..." Accordingly, the rejection should be withdrawn.

35 U.S.C. § 102

The examiner rejected claims 1-5, 7-12, 14-21, and 23-26 under 35 U.S.C. § 102(c) as being anticipated by U.S. Patent Application Publication No. 2004/0030770 ("Pandya").

As amended, claim 1 recites: "[a] method comprising...receiving a packet in a packet processor, the packet processor comprising...a stack processor...a hardware scheduler in the stack processor...a control processor; and a packet engine managed by the control processor...scheduling processing of the packet received by the packet processor with the hardware scheduler, wherein scheduling includes receiving an interrupt signal from the packet engine"

Pandya describes the following:

The DMA engine, block 2205 and the bus controller, block 2201, allow the packet engine to move the data packets from the scheduler of FIG. 19 and the host interface into the data memory 2206 for operation. The DMA engine may hold multiple memory descriptors to store/retrieve packet/data to/from host memory/packet memory. This would enable memory accesses to happen in parallel to packet processor engine operations. The DMA engine 2205 also may be used to move the data packets to and from the TCP and storage engines 2210, 2211.¹

The examiner equates the packet processor of Pandya with the stack processor of the instant claim 1. Assume *arguendo* that the DMA engine of Pandya can be equated to the control processor of the instant claim 1. In that case, for claim 1 to read on Pandya, the DMA engine of Pandya must manage a packet engine from which interrupt signals are received at the packet processor. In the passage cited by the examiner, however, Pandya describes:

The host interface controller 1710, seen in greater detail in FIG. 27, provides the configuration registers, DMA engines for direct memory to memory data transfer, the host command block that performs some of the above tasks, along with the host interface transaction controller and the host interrupt controller. The host input and output queues 1707, 1709 provide the queuing for incoming and outgoing packets.²

¹ Pandya, Paragraph [0120]

² *Id.*, Paragraph [0112]

Nowhere in this passage, or anywhere else, is Pandya understood to describe or suggest that anything managed by the DMA engine sends an interrupt signal received by the packet processor. Pandya fails to anticipate claim 1.

Independent claims 8, 15, 18, 21, and 24 have similar features and are similarly not anticipated by Pandya. Accordingly, the rejection should be withdrawn.

35 U.S.C. § 103

The examiner rejected claims 6 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Pandya in view of "Master's Thesis: Implementation of a network Processor Based Exchange Terminal", Stockholm, November 2002 ("Stenstrom"). The examiner rejected claim 22 under 35 U.S.C. § 103(a) as being unpatentable over Pandya in view of U.S. Patent Application Publication No. 2002/0083297 ("Modelski").

Claim 6 depends from claim 1, claim 13 and depends from claim 8. Claim 22 was cancelled and its feature now a feature of amended claim 21.

It was shown above that Pandya neither describes nor suggests the features of claims 1, 8, and 21. Stenstrom and Modelski were introduced to cover specific dependent claims and also fail to describe or suggest the features of claims 1, 8, and 21. Accordingly, the rejections should be withdrawn.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing remarks, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made

Applicant : Tomasz Bogdan Madajczak
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arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fee is due. Please apply any other charges or credits to deposit account 06-1050, referencing 10559-0903001.

Respectfully submitted,

Date: December 8, 2008

/Denis G. Maloney/
Denis G. Maloney
Reg. No. 29,670

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (877) 769-7945